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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,647	12/30/2003	Cheolsoo Park	20059/PIA31228	9407

34431 7590 05/04/2005

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,647	PARK, CHEOLSOO	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *December 30, 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed December 30, 2003.

Drawings

The drawings are objected to because Figure 2E is inconsistent with Figures 2A-2D. Specifically, Figure 2D shows source/drain regions 7a/7b as being in direct contact with semiconductor layer 4; however, Figure 2E shows that there is a new un-numbered layer in between the bottom of the source/drain regions 7a/7b and the semiconductor layer. Additionally, Figure 2D shows that there is a layer 3 underneath layer 5; whereas, Figure 2E does not show layer 3 but instead shows that there is a new un-numbered layer on the sides and bottom of layer 5. Also, the shading of source/drain regions in Figure 2D is different than it is in Figure 2E.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming a trench in an active region by etching the first nitride layer and a portion of the semiconductor substrate", as recited in claim 1, must be shown or the feature(s) canceled from the claim(s). The drawings do not show etching the semiconductor substrate. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The last two lines of claim 1 recite the limitation of "depositing a dielectric layer forming plugs on the source, drain, and gate." The specification does not provide antecedent basis for depositing a dielectric layer that forms plugs on the source, drain and gate.

Claim 2 recites the limitation of "depositing a shallow trench isolation (STI)." The specification does not provide antecedent basis for this limitation in the claim.

Claim 3 recites the limitation of "etching the first oxide layer to a thickness approximately equal to a thickness of the gate electrode." The specification does not provide antecedent basis for this limitation in the claim.

Claim 7 recites the limitation of "wherein the source and the drain are formed by a BSG or PSG method." The specification does not provide antecedent basis for this limitation in the claim.

The disclosure is objected to because of the following informalities:

At line 20 of page 3, the specification refers to layer (8) as "a second nitride layer". However, at lines 11-13 and 21-22 of page 4, the specification refers to layer (10) as "a second nitride layer". The specification should be amended such that layer (10) is referred to as "a third nitride layer".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant's invention, as shown in the drawings and disclosed in the detailed description of the invention in the specification is different from the invention disclosed in claims 1 and 3. Therefore, it is unclear as to which of these inventions Applicant has possession. Specifically, claims 1 and 3 recite the limitation of etching the semiconductor substrate to form a trench in the active region. Figures 2A-2E do not show *any* such trench being formed in the substrate; and the detailed description of the invention in the specification does not disclose that the substrate is *ever* etched in the active region. Additionally, claim 3 recites the limitation that the forming of the trench in the active region by etching the first nitride layer also involves etching the first

oxide layer; however, Applicant's specification and drawings disclose that the only trench formed by etching the first nitride layer is conducted *before* the first oxide layer is ever even deposited onto the substrate. Furthermore, claim 3 recites the limitation of etching the first oxide layer to a thickness approximately equal to a thickness of the gate electrode; however, the specification and drawings disclose that the first oxide is equal to a thickness of the gate electrode *as deposited*, and the first oxide is substantially less than the thickness of the gate electrode after it has been etched.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites the limitations of forming the source and drain by "a BSG or a PSG method." The specification does not disclose forming the source and drain by these methods. Furthermore, it is unclear as to what the acronyms BSG and PSG stand for, since BSG and PSG are commonly used in the semiconductor manufacturing art to serve as an acronym for boron-silicate-glass and phospho-silicate-glass; yet the specification states that the source and drain are made of epitaxial silicon.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Krivokapic (US 5,879,998).

Regarding claim 1, Krivokapic discloses depositing an isolation oxide layer (152) and a first nitride layer (120) on a semiconductor substrate (60), forming a trench in an active region by etching the first nitride layer and a portion of the semiconductor substrate, performing an epitaxial growth on the active region where the source and the drain are to be formed to thereby form the source and the drain and depositing a first oxide layer (205) on the epitaxial growth, depositing a second nitride layer (215) on the source and drain, etching a portion of the first oxide layer where a gate is to be formed using a gate mask, depositing and planarizing a third nitride layer (80) on the source, drain and active region to thereby form a nitride layer to control the length of the gate, sequentially depositing a gate isolation layer (205) and a gate electrode (240) on the active region, depositing a dielectric layer (285), and forming plugs on the source, drain and gate (col. 4, ln. 20 – col. 7, ln. 10).

Regarding claim 2, Krivokapic discloses that the isolation oxide is a shallow trench isolation (STI) (col. 5, ln. 28-36).

Regarding claim 6, Krivokapic discloses that the second nitride layer is thicker than the first oxide layer (Fig. 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic (US 5,879,998) in view of Chau et al. (US 6,165,826).

Regarding claim 4, Krivokapic discloses that the first oxide layer is etched where the source and drain are to be formed using an oxide etching step, but does not disclose any particular etchant to be used to do the etching (col. 4, ln. 13-17). Like Krivokapic, Chau discloses a process of forming transistors on a semiconductor substrate for formation of an integrated circuit thereon. Chau discloses that an etchant of a diluted HF solution can selectively etch an oxide layer relative to silicon nitride and silicon layers (col. 14, ln. 58 – col. 15, ln. 9). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a diluted HF solution to etch the oxide layer of Krivokapic because Krivokapic discloses using an oxide etching process and Chau discloses that a diluted HF solution can selectively etch oxide relative to silicon nitride and silicon.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic (US 5,879,998) in view of Wolf et al. ("Silicon Processing for the VLSI Era").

Regarding claim 5, Krivokapic does not disclose what type of etchant is used to etch the first oxide layer in the step of etching the vertical trench (22) (Fig. 2b). However, as is disclosed by Wolf, dry anisotropic etching is preferred over wet etching because dry etching avoids the problems of the handling, consumption and disposal of the relatively large quantities of dangerous acids and solvents required in wet etching (pg. 539). At the time of the invention, it

would have been obvious to one of ordinary skill in the art to use dry anisotropic etching to etch the first oxide layer during formation of the vertical trench (22) because dry etching avoids the problems of handling of dangerous chemicals that are associated with wet etching.

Claims 1, 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (US 6,872,626) in view of Shimizu et al. (US 6,066,881).

Regarding claim 1, Cheng discloses depositing an isolation oxide layer (140) and a first nitride layer (150) on a semiconductor substrate (110), forming a trench (160) in an active region by etching the first nitride layer and a portion of the semiconductor substrate, performing an epitaxial growth on the active region where the source and the drain are to be formed to thereby form the source and the drain and depositing a first oxide layer (190) on the epitaxial growth, depositing a second nitride layer (150) on the source and drain, etching a portion of the first oxide layer where a gate is to be formed using a gate mask, depositing and planarizing a third nitride layer (135) on the source, drain and active region to thereby form a nitride layer to control the length of the gate, and sequentially depositing a gate isolation layer (125) and a gate electrode (130) on the active region (col. 3, ln. 43 – col. 6, ln. 64). Cheng does not disclose the process steps involved in completing the semiconductor device, such as depositing a dielectric layer over the source, drain and gate and forming plugs therein. Like Cheng, Shimizu discloses a process of forming transistors on a semiconductor substrate for formation of an integrated circuit thereon. Shimizu discloses that after formation of the transistor gate, source and drain regions, a dielectric layer (15/17/22) is deposited over those regions and conductive plugs connecting to the gate, source and drain regions are formed therein (Fig. 1A-1B). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit a dielectric over the gate,

source and drain regions of Cheng and form plugs therein in order to provide the necessary electrical connections to the gate, source and drain regions of the transistor, as is conventional in the art and shown by Shimizu.

Regarding claim 2, Cheng discloses that the isolation oxide is a shallow trench isolation (STI) (col. 4, ln. 1-5).

Regarding claim 7, Cheng discloses that the source and drain may be formed by in-situ doping during the epitaxial growth process (col. 7, ln. 9-15).

Claims 1, 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US 6,852,559) in view of Shimizu et al. (US 6,066,881).

Regarding claim 1, Kwak discloses depositing an isolation oxide layer (17) and a first nitride layer (21) on a semiconductor substrate (11), forming a trench (23) in an active region by etching the first nitride layer and a portion of the semiconductor substrate, performing an epitaxial growth on the active region where the source and the drain are to be formed to thereby form the source and the drain and depositing a first oxide layer (19) on the epitaxial growth, depositing a second nitride layer (25) on the source and drain, etching a portion of the first oxide layer where a gate is to be formed using a gate mask, depositing and planarizing a third nitride layer (33) on the source, drain and active region to thereby form a nitride layer to control the length of the gate, and sequentially depositing a gate isolation layer (29) and a gate electrode (31) on the active region (Fig. 2A-2F; col. 2, ln. 65 – col. 4, ln. 44). Kwak does not disclose the process steps involved in completing the semiconductor device, such as depositing a dielectric layer over the source, drain and gate and forming plugs therein. Like Kwak, Shimizu discloses a process of forming transistors on a semiconductor substrate for formation of an integrated circuit

thereon. Shimizu discloses that after formation of the transistor gate, source and drain regions, a dielectric layer (15/17/22) is deposited over those regions and conductive plugs connecting to the gate, source and drain regions are formed therein (Fig. 1A-1B). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit a dielectric over the gate, source and drain regions of Kwak and form plugs therein in order to provide the necessary electrical connections to the gate, source and drain regions of the transistor, as is conventional in the art and shown by Shimizu.

Regarding claim 2, Kwak discloses that the isolation oxide is a shallow trench isolation (STI) (col. 3, ln. 13-18).

Regarding claim 6, Kwak discloses that the second nitride layer is thicker than the first oxide layer (Fig. 2d).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US 6,852,559) in view of Shimizu et al. (US 6,066,881) as applied to claim 1 above, and further in view of Chau et al. (US 6,165,826).

Regarding claim 4, Kwak discloses that the first oxide layer is etched where the source and drain are to be formed using a wet etching step, but does not disclose any particular etchant to be used to do the etching (col. 4, ln. 13-17). Like Kwak, Chau discloses a process of forming transistors on a semiconductor substrate for formation of an integrated circuit thereon. Chau discloses that an etchant of a diluted HF solution can selectively etch an oxide layer relative to silicon nitride and silicon layers (col. 14, ln. 58 – col. 15, ln. 9). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a diluted HF solution to etch

the oxide layer of Kwak because Kwak discloses using a wet etching process and Chau discloses that a diluted HF solution can selectively etch oxide relative to silicon nitride and silicon.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US 6,852,559) in view of Shimizu et al. (US 6,066,881) as applied to claim 1 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI Era").

Regarding claim 5, Kwak does not disclose what type of etchant is used to etch the first oxide layer in the step of etching the vertical trench (22) (Fig. 2b). However, as is disclosed by Wolf, vertically profiled etches such as that shown in Figure 2b of Kwak are done with an anisotropic process that can etch in a longitudinal direction faster than in a horizontal direction (pg. 539-541). Furthermore, dry anisotropic etching is preferred over wet etching because dry etching avoids the problems of the handling, consumption and disposal of the relatively large quantities of dangerous acids and solvents required in wet etching (pg. 539). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use dry anisotropic etching to etch the first oxide layer during formation of the vertical trench (22) because anisotropic (directional) etching is required to form the steep straight walls of the trench and because dry etching avoids the problems of handling of dangerous chemicals that are associated with wet etching.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
April 27, 2005

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